486-GIO-VP

MAIN BOARD
User's Guide

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Chapter 1

Overview

Based on an ISA/VL-bus, the 486-GIO-VP mainboard empowers any high-end system to exploit a wide-range of hardware and software capabilities and applications. The board's special feature is the VIA GMC chipset, a highly integrated single chipset that supports write-back and SMM (System Management Mode) CPUs, multi-master operations and provides built-in power management features ideal for Green PCs. This chapter gives you a brief overview of this mainboard, providing basic information on its major parts and components.

Specifications

The 486-GIO-VP mainboard comes with the following features:

- Supports Intel 80486SX/DX/DX2/P24T/486S-series/ CX486S™ CPU microprocessor in PGA packages.
- VIA GMC VT82C486A PC/AT chipset includes built-in 8042 keyboard controller.
- Award BIOS.
- Supports 64/128/256K direct-mapped write-back/write-through cache memory.
- 30 - and 72 - pin SIMM sockets supports 1 up to 96MB DRAM for 486 system and provides page mode DRAM operation.
- Supports system and video BIOS cacheable and shadow.
- Supports decoupled DRAM refresh.
- Optional built-in ZIF socket that accepts Intel's OverDrive™ processors.
- Six 16-bit ISA expansion slots.

- Supports two VESA bus slots for Local bus master or slave.
- Dallas DS12885Q/VIA VT82885V real time clock/calendar.
- Built-in IDE HDD/FDD and Local Bus IDE interface.
- Two serial / one parallel ports.
- Promise PDC20230 Local Bus IDE Controller (optional)
- Provides built-in power management features ideal for Green PCs.
- Flash ROM (Optional).

Mainboard Layout

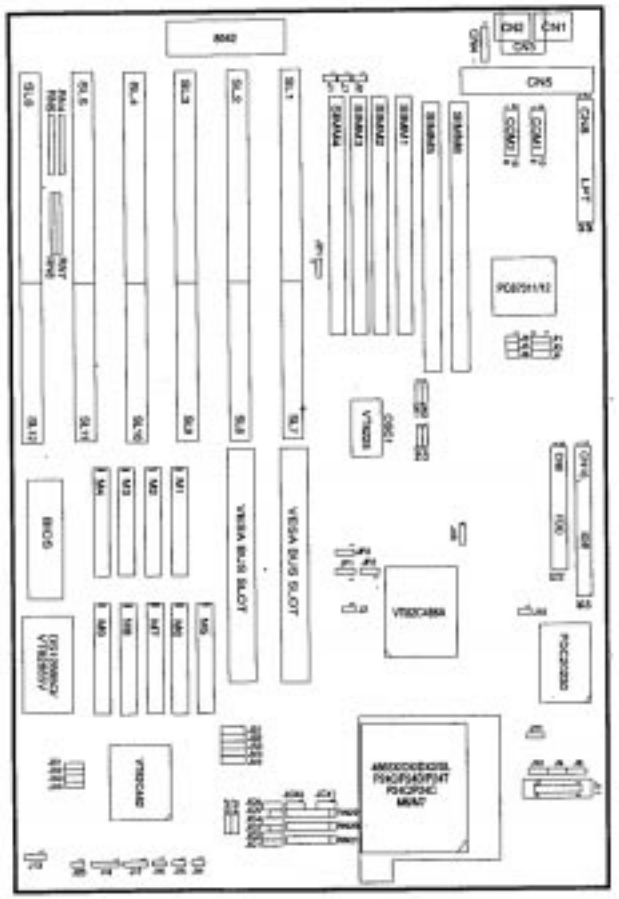


Figure 1-1. Mainboard Layout

System Block Diagram

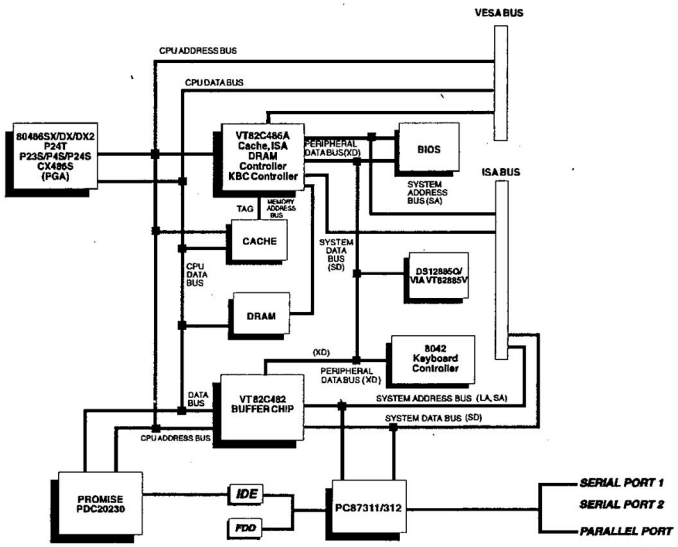


Figure 1-2. System Block Diagram

Chapter 2

Mainboard Settings

The 486-GIO-VP has several user-adjustable jumpers and connectors on the board that allow you to configure your system to suit your every need. This chapter contains information on the various jumper and connector settings you can make on your mainboard.

Jumpers

Jumpers are used to select the operation modes for your system. Some jumpers on the board have three metal pins with each pin representing a different function. To "set" a jumper, a black cap containing metal contacts is placed over the jumper pin/s according to the required configuration. A jumper is said to be "shorted" when the black cap has been placed on one or two of its pins, as shown in the figure below:

Figure 2 - 1 Jumper with Pins Shorted

CPU Selector Jumpers

To allow your system to be used with a variety of CPU's, 486-GIO-VP provides jumpers that can be set according to the CPU you want installed. Follow the diagrams found in the lower-middle area of the board to determine the proper arrangement for the CPU you are using.

The next tables summarizes the settings of the CPU Selector jumpers:

JUMPER	486SX/ P23S*	Am486DXL P24S*/P4S*/ DX4 486DX/ IntelDX2™	P24CT/P24T	Cx486S (M6)	Cx486DX (M7) Cx486S+ Cx487S (M6+C6)	P24D*
JC1, JC2	2-3	1-2	1-2	2-3	1-2	1-2
JC3	open	open	shorted	open	open	open
JC4	1-2	1-2	2-3	1-2	1-2	2-3
JC7	shorted	shorted	shorted	open	open	shorted

*P23S,P24S, and P4S are the SL-enhanced CPUs while P24T is the Pentium Overdrive Processor.

JUMPER (RP 0Ω 8 p4R)	P23S/P4S/ P24S/P24T	486DX/DX2 /SX	Cx486S/DX	DX4/P24D/ P24CT	Am486DXL
JC5	shorted	open	open	shorted	open
RN20	empty	empty	inserted	empty	empty
RN21	empty	empty	empty	inserted	empty
RN22	empty	empty	empty	empty	inserted

JC6	DX4 CLOCK MODE
1-2	2X
2-3	2.5X
empty	3X

P24T	WRITE BACK	WRITE THROUGH
JT1	1-2	2-3

JCX1,JCX2	S-SERIES TYPE
Intel	1-2
Cyrix	2-3

	JX2	JP2
IRQ15 (Regular CPUs - - Default)	1-2	1-2
*SMI (Cyrix or Intel S-series CPUs)	2-3	2-3

*IRQ15 is no longer available for the other devices when SMI is selected.

Table 2 - 1 Jumper Settings for CPU Selector

→ **NOTE : Users are not encouraged to change the jumper settings not listed in this manual as they are considered factory defaults which may adversely affect system performance.**

JUMPER	DESCRIPTION
J1	Disable Outlet
J2	Display type open-Mono/EGA/VGA Short - color
J3	ISA Master Transfer Rate Short- - - For≥ 5.7 $^{MB}/_{sec}$ Open —for 5.0 $^{MB}/_{sec}$
J4	Short - - - IDE Connector Pin 27 Link To IOCHRDY Signal
	Open - - - IDE Connector Pin 27 Open
J5	Short- - - IDE Connector Pin 28 Link To BALE Signal
	Open - - - IDE Connector Pin 28 Open
J6	IDE LED
J7	Short - - - Clear Password
	Open - - - default
J14	Standard Turbo LED
J15	Turbo SWITCH
J16	Reset
J17	Speaker
J18	Power LED & Keylock
J19	Hardware Sleep
J20	Green Status LED
J21	1-2 Always Short
JP3	1-2 Always Short
JF	1-2 Always Short
JX1	1-2 Always Short

Table 2-2. JumperDescription

Printer port direction Jumper

DIRECTION	OUTPUT	INPUT	BIDIRECTION
JG	1-2 (default)	1-2	2-3
JH	2-3 (default)	1-2	Don"t Care

Table 2 - 3. Printer port direction jumper

KBC Selection

JUMPER	INTERNAL K/B CONTROLLER & PS/2 MOUSE	INTERNAL K/B CONTROLLER W/O MOUSE	EXTERNAL K/B CONTROLLER
JX3	2-3	2-3	1-2
JX4	2-3	1-2	1-2
RN4	Off	Off	On
RN5	Off	On	Off
RN8	On	Off	Off
RN7	Off	Off	On

Table 2-4. Jumper Description

CPU Clock VIA (JK1 - JK4)

CLK 2	JK1	JK2	JK3	JK4
25 MHz	2-3	1-2	2-3	1-2
33.3 MHz	2-3	2-3	1-2	1-2
40 MHz	1-2	1-2	2-3	1-2
50 MHz	2-3	1-2	2-3	2-3

Table 2-5. CPU Clock VIA Jumper Selection (JK1.1 - JK1.4)

Connectors

The connectors allow the mainboard to connect electronically with other parts of the system. Some connectors have two pins, others have four or five pins. Some malfunction problems encountered with your system may be caused by loose or improper connections. Ensure that all connections are in place and firmly attached.

CONNECTOR	PIN OUTS	SIGNAL NAME
CN1 PS/2 Keyboard Connector	1 2, 6 3 4 5	Keyboard data NC Ground +5V Keyboard clock
CN2 PS/2 Mouse Connector	1 2, 6 3 4 5	Mouse data NC Ground +5V Mouse clock
CN3 At Keyboard Connector	1 2 3 4 5	Keyboard clock Keyboard data NC Ground +5V
CN4 PS/2 MOUSE Pin Connector	1 2 3 4 5	Mouse data NC Ground +5V Mouse clock
CN5 Power Connector	1 2, 10, 11, 12 3 4 5, 6, 7, 8 9	Power good +5V +12V –12V Ground –5V
J6 HDD_LED Connector	1 2	LED- LED+
J11 3.3V daughter board Connector	1, 3, 14, 16 2, 4, 13, 15 5, 12 6 7, 8, 9, 10 11	+3.3V +5V Voltage Switch signal NC Ground +12V
J13 External Battery Connector	1 2, 3 4	Anode+ NC Cathode –
J14 Turbo LED	1 2	LED+ LED-

J15 Turbo Switch	1 2	Turbo Signal Ground
J16 Hardware Reset	1 2	Ground Reset signal
J17 Speaker Connector	1 2 3 4	Speaker signal NC Ground +5V
J18 Keylock and Power LED Connector	1 2 3, 5 4	Power LED signal Spare Ground Keylock

Table 2-6. Connector Pin Definitions

VESA Bus Connector

The cache system board provides two high-performance VESA bus connectors, SL13 and SL14, for use with VESA peripherals. These connectors can be utilized for one Local Bus Master and one Local Bus Slave, either (SL13) or (SL14).

The following tables give the pin assignments for SL13 and SL14. Side A of the connector are pin outs on the board's component side while Side B are pin outs on the board's solder side. Jumpers JV2 and JV3 give more information on settings on the mainboard and the VL-bus controller.

JUMPER	PIN	DESCRIPTION
JV2	1-2	> 33MHz
	2-3	< or = 33MHz
JV3	1-2	1 WAIT WRITE
	2-3	0 WAIT WRITE

Table 2 - 7. VESA Bus Connector

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL13 — Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV1#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK1
			58	LBS16#

Table 2-8 . Local Bus Connector Pin Assignment (Continued)

CONNECTOR	SIDE A - PINS AND PIN OUTS		SIDE B - PINS AND PIN OUTS	
SL14— Local Bus Connector	01	DAT01	01	DAT00
	02	DAT03	02	DAT02
	03, 10, 17, 24, 35, 43, 51	Ground	03	DAT04
	04	DAT05	04	DAT06
	05	DAT07	05	DAT08
	06	DAT09	06, 14, 22, 29, 38, 49, 55	Ground
	07	DAT11	07	DAT10
	08	DAT13	08	DAT12
	09	DAT15	09, 20, 32, 57	VCC
	11	DAT17	10	DAT14
	12, 27, 40, 53	VCC	11	DAT16
	13	DAT19	12	DAT18
	14	DAT21	13	DAT20
	15	DAT23	15	DAT22
	16	DAT25	16	DAT24
	18	DAT27	17	DAT26
	19	DAT29	18	DAT28
	20	DAT31	19	DAT30
	21	ADR30	21	ADR31
	22	ADR28	23	ADR29
	23	ADR26	24	ADR27
	25	ADR24	25	ADR25
	26	ADR22	26	ADR23
	28	ADR20	27	ADR21
	29	ADR18	28	ADR19
	30	ADR16	30	ADR17
	31	ADR14	31	ADR15
	32	ADR12	33	ADR13
	33	ADR10	34	ADR11
	34	ADR08	35	ADR09
	36	ADR06	36	ADR07
	37	ADR04	37	ADR05
	38	WBACK#	39	ADR03
	39	BE0#	40	ADR02
	41	BE1#	41	NC
	42	BE2#	42	RESET#
	44	BE3#	43	D/C#
	45	ADS#	44	M/IO#
	48	LRDY#	45	W/R#
	49	LDEV0#	48	RDYRTN#
	50	LREQ#	50	IRQ9
	52	LGNT#	51	BRDY#
	54, 55, 56	ID2, 3, 4	52	BLAST#
	57	LKEN#	53, 54	ID0, 1
	58	LEADS#	56	LCLK0
			58	LBS16#

Table 2-8. Local Bus Connector Pin Assignment

Local Activity Jumper

JV4	JV5
1-2 (default)	1-2 (default)
2-3 If Local VGA or Local IDE plug in SL14	2-3 If Local VGA or Local IDE plug in SL13

Table 2 - 9. Local Activity Jumper

Local IDE Speed

	J8	J9
FAST	1-2	1-2
MEDIUM	1-2	2-3
NORMAL	2-3	2-3

Table 2-10. Local IDE Speed

Local IDE

JUMPER	PIN	DESCRIPTION
J10	1-2	ENABLE
	2-3	DISABLE

Table 2-11. Local IDE

Installing DRAM

SIMM Banks

The 486-GIO-VP can accommodate on-board memory from 1 to 96MB using SIMMs (Single-In-Line Memory Modules). The mainboard has three memory banks — Bank 0, 1, 2. Each bank can accept either a 256KB, IMB, 4MB, or 16MB SIMM in each socket.

DRAM Configuration

Memory can be installed in a variety of configurations, as shown in the next table:

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
1MB	256K x 4		
		1M x 1	
			1M x 1
2MB	256K x 4	1M x 1	
		1M x 1	1M x 1
	256K x 4		1M x 1
3MB	256K x 4	1M x 1	1M x 1
4MB	1M x 4		
		4M x 1	
			4M x 1
5MB	256K x 4	4M x 1	
	256K x 4		4M x 1
	1M x 4	1M x 1	
	1M x 4		1M x 1
		1M x 1	4M x 1
		4M x 1	1M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
6MB	256K x 4	4M x 1	1M x 1
	256K x 4	1M x 1	4M x 1
	1M x 4	1M x 1	1M x 1
8MB	1M x 4	4M x 1	
	1M x 4		4M x 1
		4M x 1	4M x 1
9MB	256K x 4	4M x 1	4M x 1
	1M x 4	1M x 1	4M x 1
	1M x 4	4M x 1	1M x 1
12MB	1M x 4	4M x 1	4M x 1
16MB	4M x 4		
		16M x 1	
			16M x 1
17MB	256K x 4	16M x 1	
	256K x 4		16M x 1
		1M x 1	16M x 1
		16M x 1	1M x 1
	4M x 4	1M x 1	
	4M x 4		1M x 1
18MB	256K x 4	1M x 1	16M x 1
	256K x 4	16M x 1	1M x 1
	4M x 4	1M x 1	1M x 1
20MB	1M x 4	16M x 1	
	1M x 4		16M x 1
	4M x 4	4M x 1	
	4M x 4		4M x 1
		4M x 1	16M x 1
		16M x 1	4M x 1

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
21MB	256K x 4	4M x 1	16M x 1
	256K x 4	16M x 1	4M x 1
	1M x 4	1M x 1	16M x 1
	1M x 4	16M x 1	1M x 1
	4M x 4	1M x 1	4M x 1
	4M x 4	4M x 1	1M x 1
24MB	1M x 4	4M x 1	16M x 1
	1M x 4	16M x 1	4M x 1
	4M x 4	4M x 1	4M x 1
32MB	4M x 4	16M x 1	
	4M x 4		16M x 1
		16M x 1	16M x 1
		32Mx1*	
			32Mx1*
33MB	256K x 4	16M x 1	16M x 1
	4M x 4	1M x 1	16M x 1
	4M x 4	16M x 1	1M x 1
36MB	1M x 4	16M x 1	16M x 1
	4M x 4	4M x 1	16M x 1
	4M x 4	16M x 1	4M x 1
48MB	4M x 4	16M x 1	16M x 1
64MB	16M x 4		
		32Mx1*	32Mx1*
65MB	16M x 4	1M x 1	
	16M x 4		1M x 1
66MB	16M x 4	1M x 1	1M x 1
68MB	16M x 4	4M x 1	
	16M x 4		4M x 1
69MB	16M x 4	1M x 1	4M x 1
	16M x 4	4M x 1	1M x 1

*Double-RAS SIMM

Table 3-1. DRAM Configurations (Continued)

TOTAL MEMORY	BANK 0 (30-PIN)	BANK 1 (72-PIN)	BANK 2 (72-PIN)
72MB	16M x 4	4M x 1	4M x 1
80MB	16M x 4	16M x 1	
	16M x 4		16M x 1
81MB	16M x 4	1M x 1	16M x 1
	16M x 4	16M x 1	1M x 1
84MB	16M x 4	4M x 1	16M x 1
	16M x 4	16M x 1	4M x 1
96MB	16M x 4	16M x 1	16M x 1

Table 3-1. DRAM Configurations

NOTE : When using double-sided SIMM, it is advised that Bank 2 be used instead of Bank 1. If Bank 1 contains a double-RAS SIMM, then Bank 0 (30-pin) is rendered inoperative.

Installation Instructions

NOTE : Always observe static electricity precautions. See "Handling Precautions" at the start of this manual.

1. Locate the SIMM banks on the mainboard. Determine your desired configuration to be installed.
2. Insert the SIMM edge connector at a 90-degree angle onto the socket.

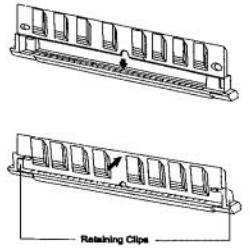


Figure 3-2. Installing SIMMs

3. Carefully push the SIMM down and back into the socket until the retaining clips of the socket snap, holding the SIMM in place. The holes in the SIMM should match the pins on the socket's retaining clips.

To remove the SIMM/s, pull the retaining latch on both ends of the socket and reverse the procedure above.

Cache Memory

The 486-GIO-VP can accept cache memory of 64, 128 or 256KB.

→ **NOTE : Be sure to use the correct chips for the amount of cache memory you want to add. You must install both the correct Cache and Tag SRAM.**

Installing Cache Memory

→ **NOTE : Always observe static electricity precautions. See "Handling Precautions" at the beginning of this manual.**

If you do not have the confidence to make the installation, better consult a service technician for assistance.

1. Locate the cache memory on the mainboard. See Figure 3-1 again.
2. Be guided by the Cache SRAM settings depending on your desired SRAM configuration.

Correct orientation of the chips is necessary for the cache to operate properly. Normally, the chips have either a curved notch or a dot. This marker on the chip must be matched to the marker on the socket for correct alignment.

Install the chips individually as follows:

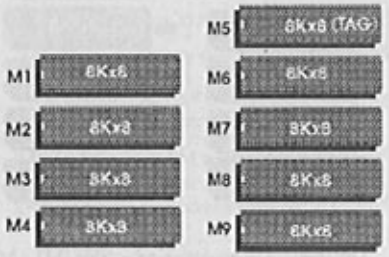
3. Align the chip with the marker on the socket. Press the chip onto the socket, ensuring that the pins on the chip are aligned with the corresponding connections on the socket.
4. Carefully apply enough pressure to partially seat the chip into the socket.

Ensure that all pins are properly aligned with the connectors and that there are no bent pins. If there are any bent pins, remove the chip, straighten the pin and repeat the process.

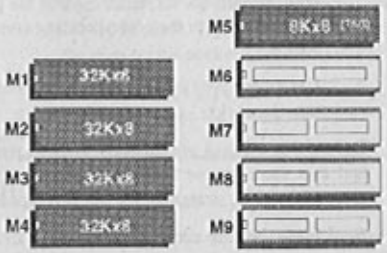
5. Press the chip completely into the socket so that the pins are properly seated.

Cache SRAM Specifications and Settings

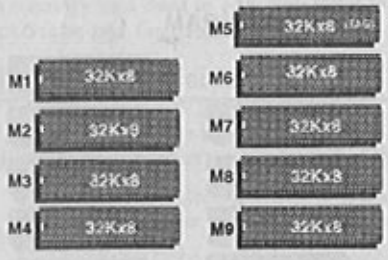
64K Cache SRAM



128K Cache SRAM



256K Cache SRAM



The cache size is jumper selectable. M1 - M4 are assigned as Bank 0 and M6 - M9 are assigned as Bank 1.

	64K	128K	256K
Bank 0	8K x 8	32K x 8	32K x 8
Bank 1	8K x 8	Empty	32K x 8
Tag RAM (M5)	8K x 8	8K x 8	32K x 8
JS1 (Jumper)	1-2	1-2	2-3
JS2 (Jumper)	1-2	2-3	2-3
JS3 (Jumper)	1-2	2-3	1-2

Table 3-2. Cache Configuration Size

Chapter 4

Award BIOS Setup

The 486-GIO-VP comes with the Award BIOS chip that contains the ROM Setup information of your system. This chip serves as an interface between the CPU and the rest of the mainboard's components. This chapter explains the information contained in the Setup program and tells you how to modify the settings according to your system configuration.

System Setup

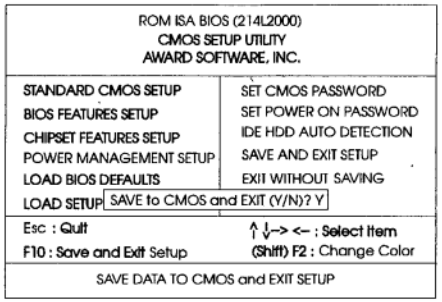
A Setup program, built into the system BIOS, is stored in the CMOS RAM that allows the configuration settings to be changed. This program is executed when:

1. User changes system configuration.
2. User changes system backup battery.
3. System detects a configuration error and asks the user to run the Setup program.

After power-on RAM testing, the message "**Press <DEL> to enter Setup**" appears. After pressing the afore mentioned keys, the following screen appears:

ROM ISA BIOS (2I4L2000) CMOS SETUP UTILITY AWARD SOFTWARE, INC.	
STANDARD CMOS SETUP BIOS FEATURES SETUP CHIPSET FEATURES SETUP POWER MANAGEMENT SETUP LOAD BIOS DEFAULTS LOAD SETUP DEFAULTS	SET CMOS PASSWORD SET POWER ON PASSWORD IDE HDD AUTO DETECTION SAVE AND EXIT SETUP EXIT WITHOUT SAVE
Esc : Quit F10 : Save and Exit Setup	↑ ↓-> <- : Select Item (Shift) F2 : Change Color
Time, Date, Hard Disk Type	

Exiting Setup



After you have made changes under Setup, press **<Esc>** to return to the main menu. Move cursor to "**Save and Exit Setup**" or press "**F10**" and then press "**Y**" to change the CMOS Setup. If you did not change anything, press **<Esc>** again or move cursor to "**Exit Without Saving**" and press "**Y**" to retain the Setup settings.

→ **NOTE : Default values of the various Setup items on this chapter may not necessarily be the same ones shown on your screen.**

Hard Disk Specifications

This appendix contains some technical information about the different IDE hard disks drives which can be installed with your 486-GIO-VP motherboard.

CONNER

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
CP-30104	120MB	726	8	39
CP-30174	170MB	903	8	46
CP-30204	200MB	683	16	38
CP-30254	251MB	895	10	55
CP-30344	343MB	904	16	46
CP-30364	360MB	702	16	63
CP-30544	544MB	1024	16	63

MAXTOR

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
7120A	120MB	1023	14	17
7170A	170MB	984	10	34
7213A	213MB	683	16	38
7245A	245MB	967	16	31
7345A	345MB	790	15	57

QUANTUM

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
LPS120AT	120MB	901	5	53
LPS240AT	240MB	723	13	51
ELS127AT	127MB	919	16	17
ELS170AT	170MB	1011	15	22

SEAGATE

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
ST3144A	125MB	1001	15	17
ST3283A	245MB	978	14	35

WESTERN DIGITAL

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
AC2120	125MB	872	8	35
AC2200	200MB	989	12	35
AC2250	255MB	1010	9	55
AC2340	341MB	1010	12	55

PRIAM

MODEL	CAPACITY	CYLINDER	HEAD	SECTOR
S19	152MB	1024	15	17